AP21088 - FrameBuffer Demo

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Rev	Who	Date	Description
Rev 0.0	pzipp	01/14/2014	Initial schematic for CameraLink Demo replacement
Rev 0.1	pzipp	03/07/2014	Switched from Arria 5 to Stratix 4, similar to PIB
Rev 0.2	pzipp	03/12/2014	- Swapped DDR banks for easier layout - Organized the inputs/outputs to Meticom devices
Rev 0.3	jwrede	05/05/2014	Added GX connectors and signals
Rev 0.4	jwrede	07/01/2014	Added bypass caps. Misc part number changes.
Rev 0.5	jwrede	07/08/2014	Misc part number changes.
Rev 1.0	jwrede	10/23/2014	I2C and LED pull-up resistor values changed. Added resistors to allow Meticom signal inversion and DDR3 I2C readback.
Rev 1.1	jwrede	10/29/2014	Changed FPGA EEPROM to 128Mb Aligned SER_TX_HS polarity
Rev 1.2	jwrede	12/04/2014	Changed U30 to LT6700-3

Aptina IMAGING

Title: Title		
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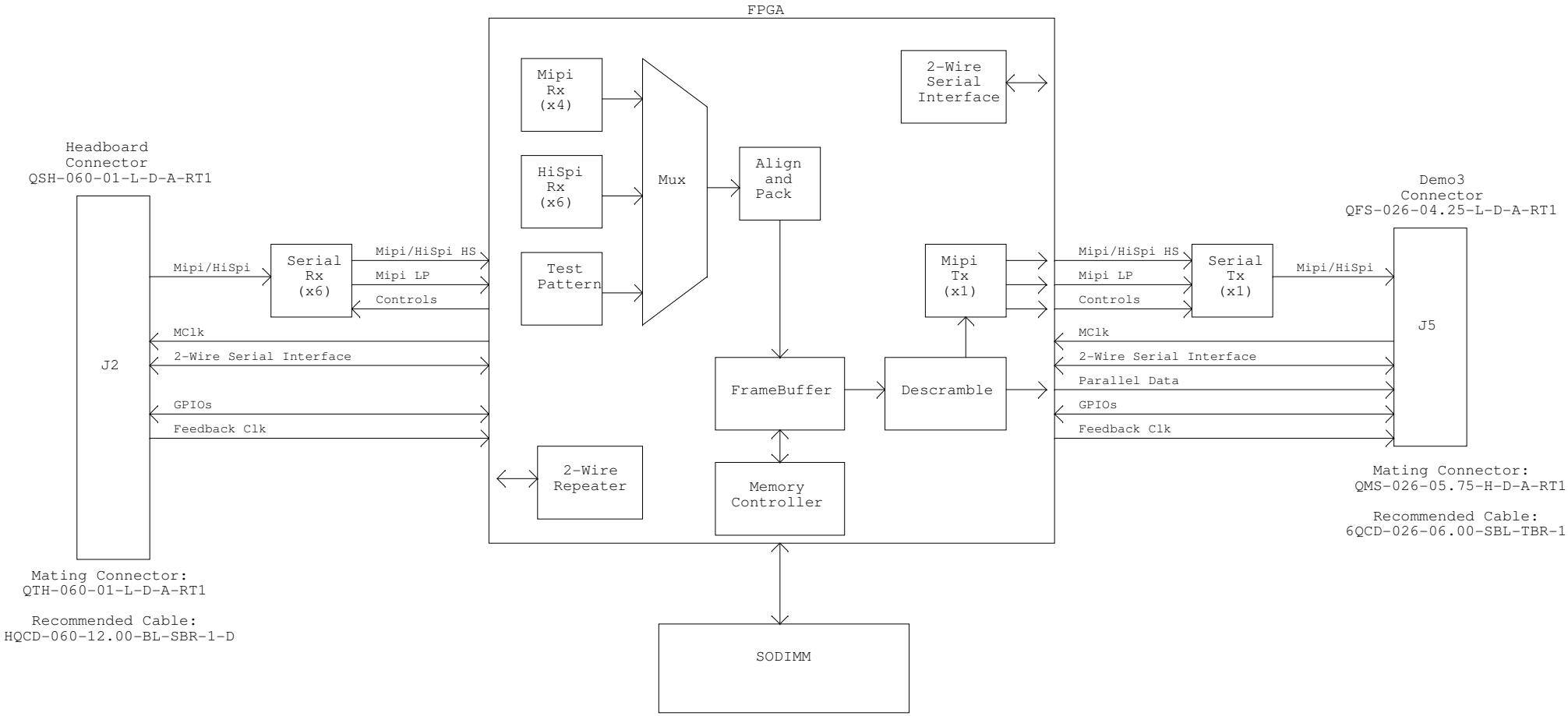
Script NOT executed



Script NOT executed

Title: Block Diagram		
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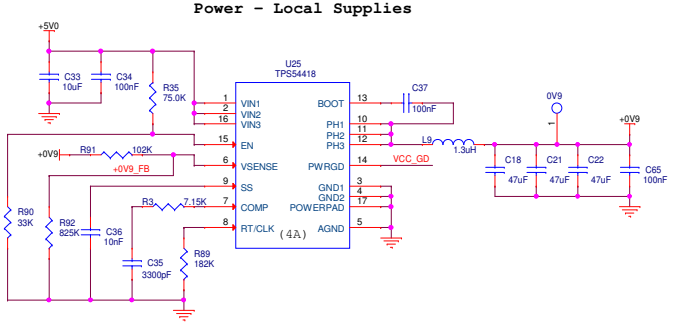
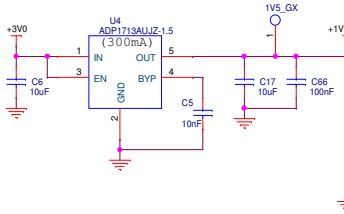
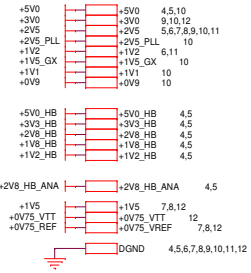
+0V9 = 2500mA (4000mA)
+1V5_GX = 220mA (300mA)

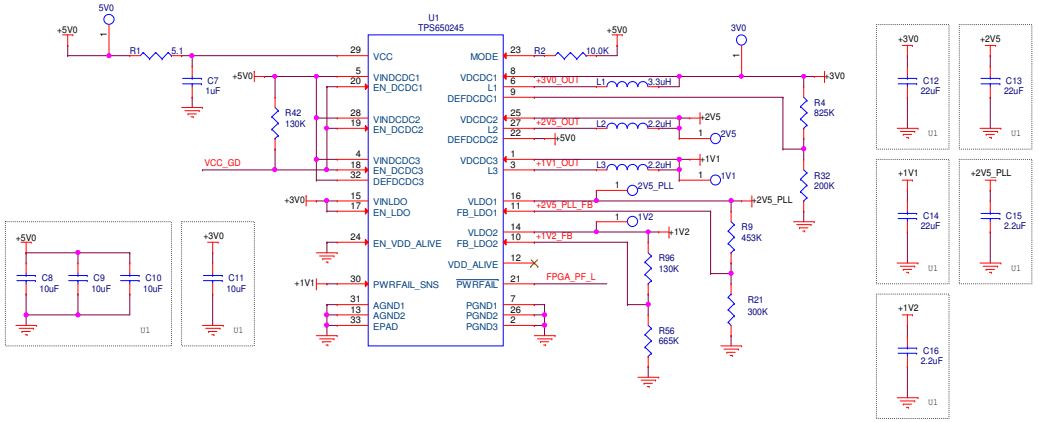
+3.0V = 650mA (1000mA)
+2.5V_PLL = 500mA (800mA)
+1.1V = 565mA (800mA)
+2.5V = 22mA (200mA)
+1.2V = 6x10mA + 1x20mA = 80mA (200mA)

Power - Local Supplies

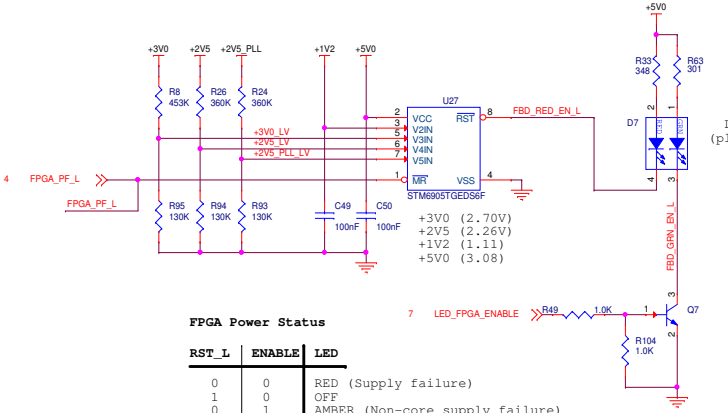








Power Monitor - Local Supplies

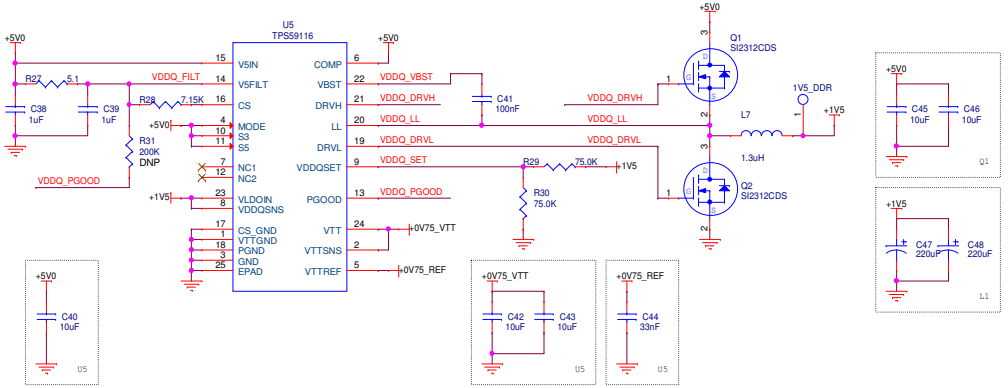


Label "FBD PWR"
(place on Bottom)

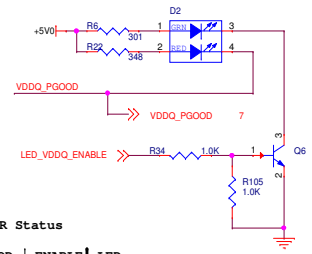
FPGA Power Status

RST_L	ENABLE	LED
0	0	RED (Supply failure)
1	0	OFF
0	1	AMBER (Non-core supply failure)
1	1	GREEN (Disable option)

Power - SODIMM



Label "DDR"
(place on Bottom)



DDR Status

PGOOD	ENABLE	LED
0	0	RED (Supply failure)
1	0	OFF
0	1	AMBER (Calibration failure)
1	1	GREEN (Disable option)

Aptina IMAGING

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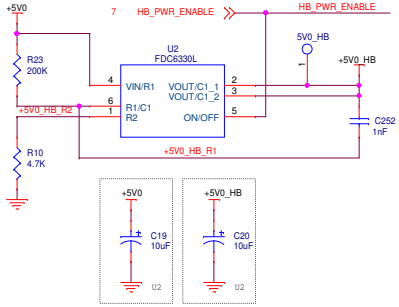
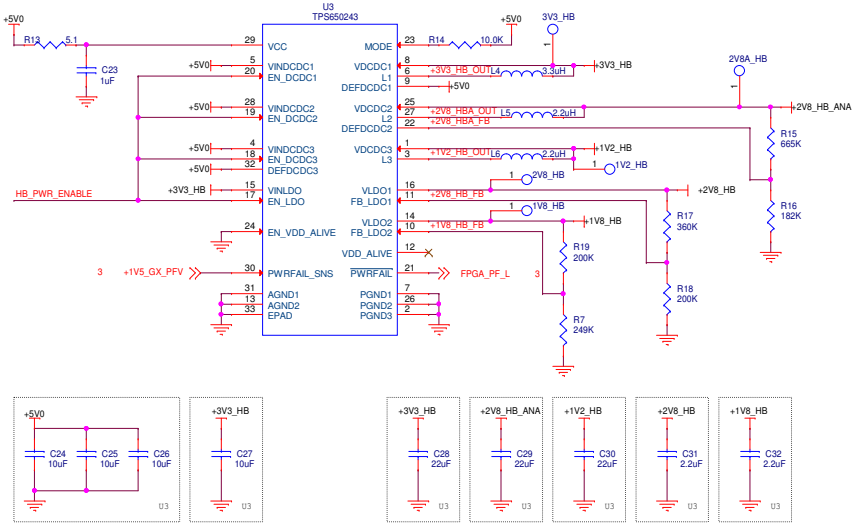
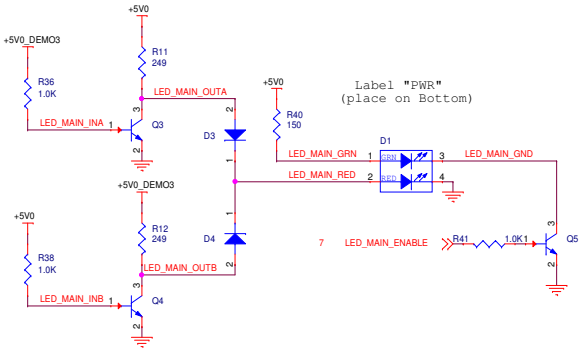
Script NOT executed

+3.3V HB = 300mA (1600mA)
+2.8V HB_ANA = 300mA (1000mA)
+1.2V HB = 300mA (800mA)
+2.8V HB = 150mA (200mA)
+1.8V HB = 150mA (200mA)

Power - Headboard Supplies





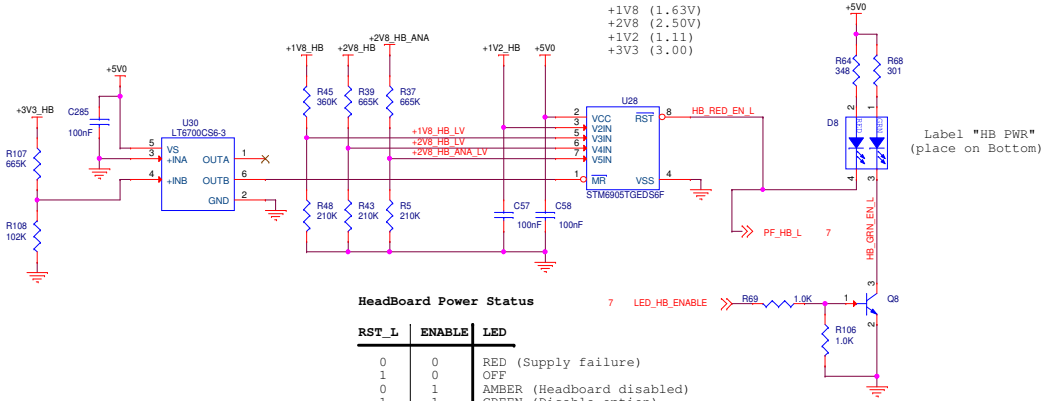


Label "PWR"
(place on Bottom)

+5V0_DEMO3	+5V0	LED
0	0	OFF
0	1	AMBER
1	0	RED
1	1	GREEN (Disable option)

Power Monitor - Headboard Supplies

+1V8 (1.63V)
+2V8 (2.50V)
+1V2 (1.11)
+3V3 (3.00)



Label "HB PWR"
(place on Bottom)

HeadBoard Power Status

RST_L	ENABLE	LED
0	0	RED (Supply failure)
1	0	OFF
0	1	AMBER (Headboard disabled)
1	1	GREEN (Disable option)

Aptina IMAGING

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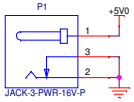
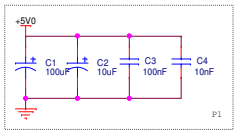
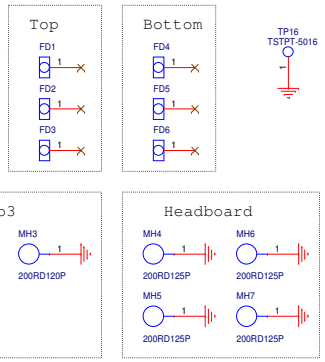
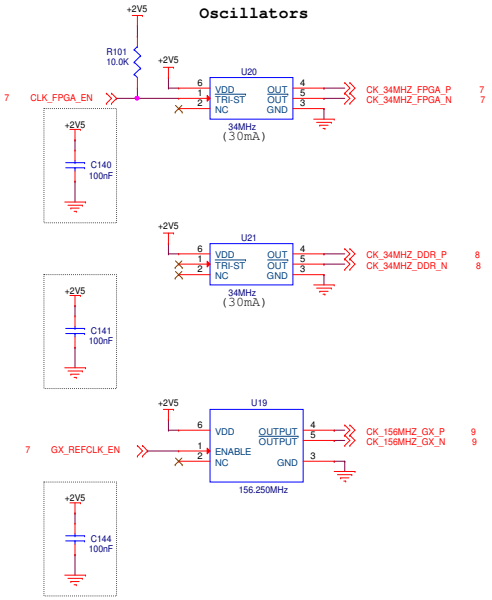
Power Input



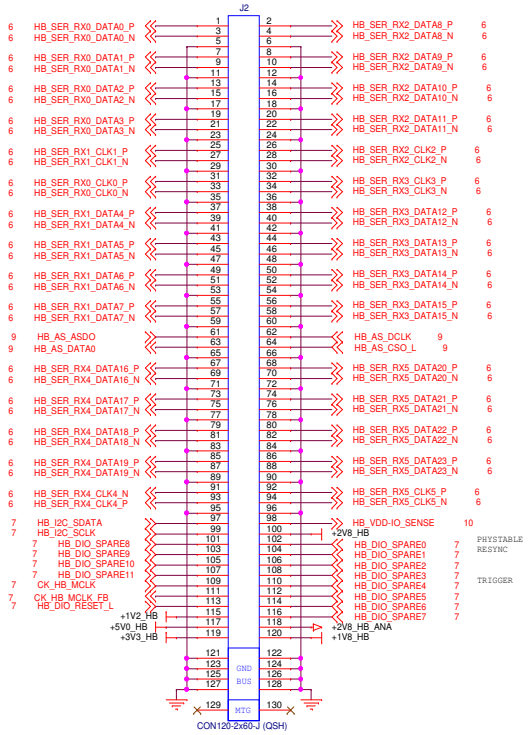




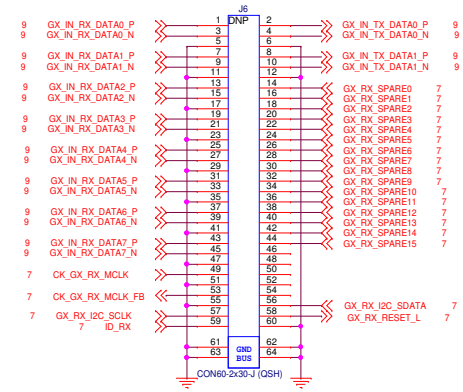
Oscillators



Headboard Connector

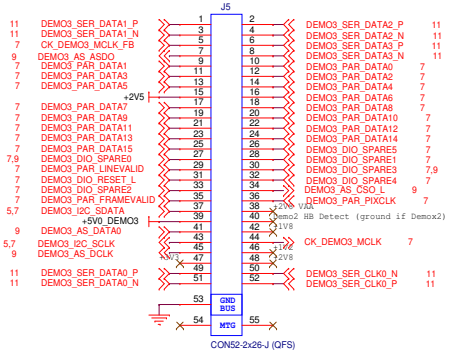


GX Receive

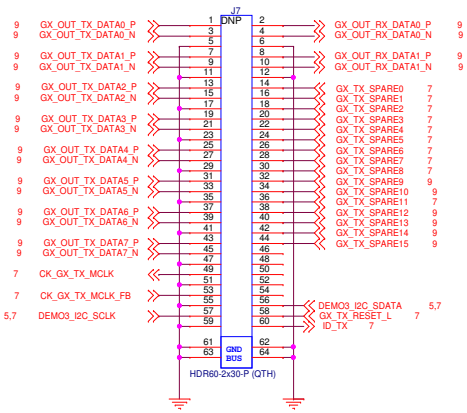


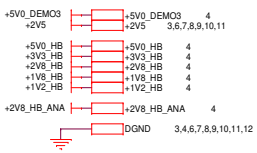
female top

Demo3 Connector



GX Transmit





Script NOT executed

Aptina IMAGING

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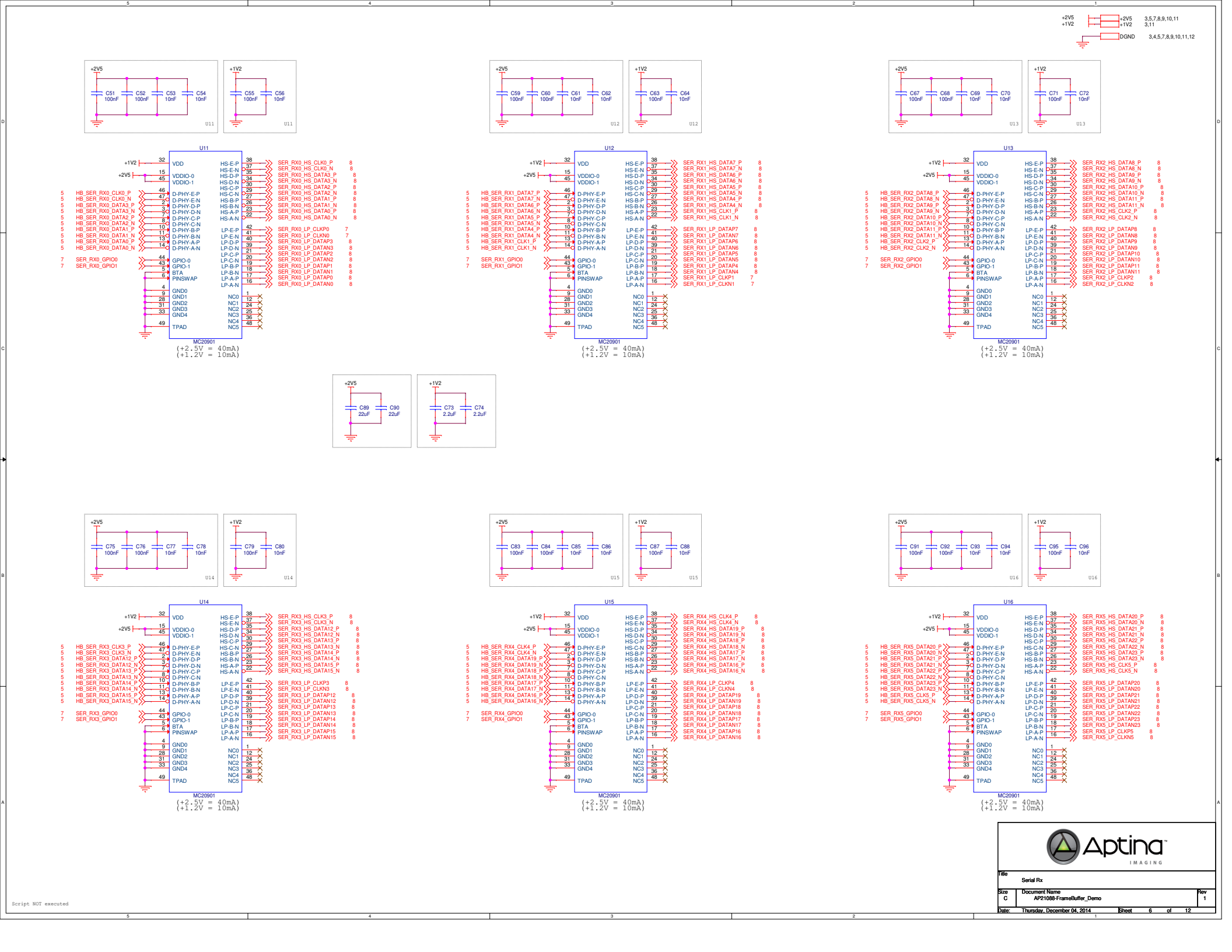
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+1V2 +1V2 3,11
DGND 3,4,5,7,8,9,10,11,12
U11
C51 100nF
C52 100nF
C53 10nF
C54 10nF
C55 100nF
C56 10nF
U12
C59 100nF
C60 100nF
C61 10nF
C62 10nF
C63 100nF
C64 10nF
U13
C67 100nF
C68 100nF
C69 10nF
C70 10nF
C71 100nF
C72 10nF
MC20901
(+2.5V = 40mA)
(+1.2V = 10mA)
C89 22uF
C90 22uF
C73 2.2uF
C74 2.2uF
U14
C75 100nF
C76 100nF
C77 10nF
C78 10nF
C79 100nF
C80 10nF
U15
C83 100nF
C84 100nF
C85 10nF
C86 10nF
C87 100nF
C88 10nF
U16
C91 100nF
C92 100nF
C93 10nF
C94 10nF
C95 100nF
C96 10nF
Script NOT executed
Aptina IMAGING
Title
Serial Rx
Size C
Document Name AP21088-FrameBuffer_Demo
Rev 1
Date: Thursday, December 04, 2014
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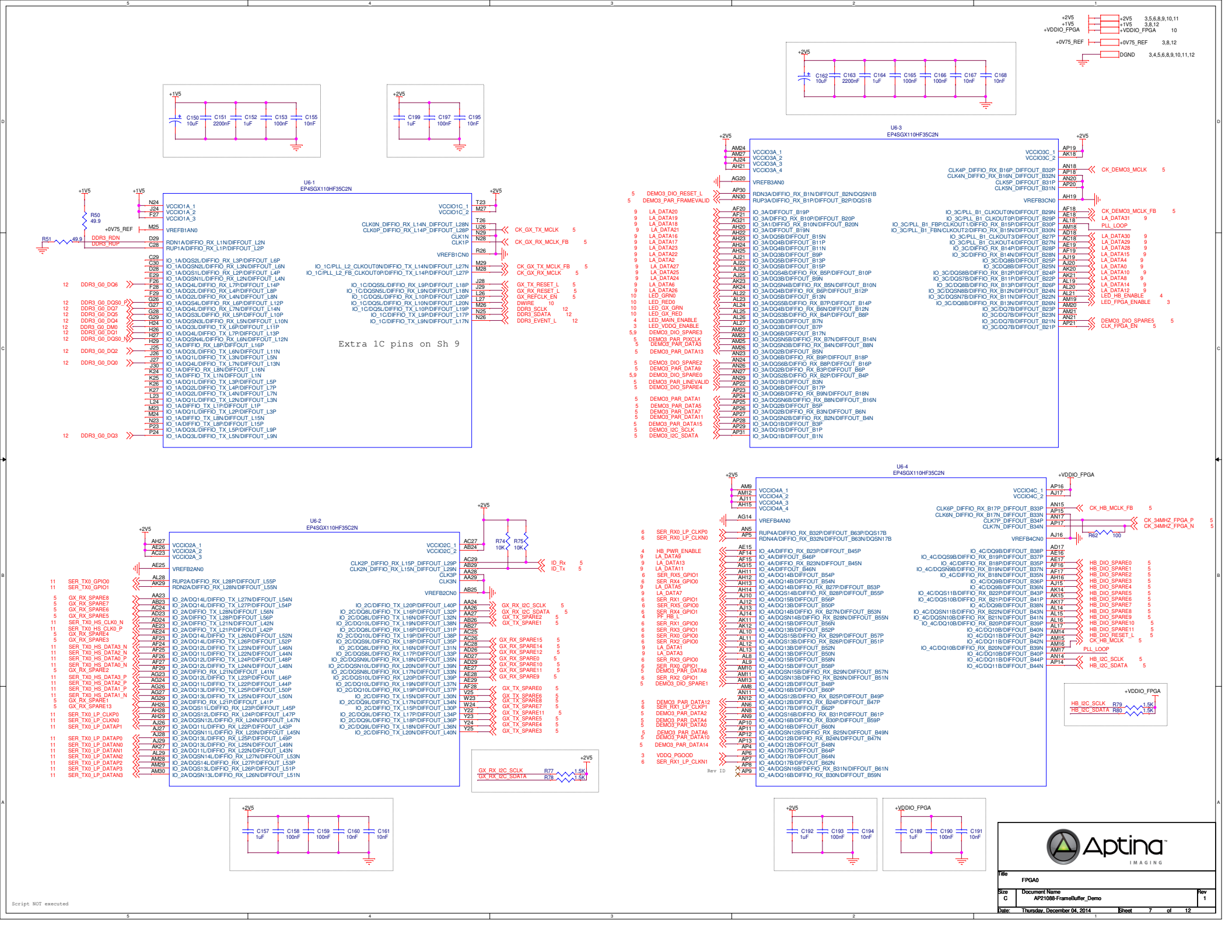
+2V5 +2V5 3,5,6,8,9,10,11
+1V5 +1V5 3,8,12
+VDDIO_FPGA +VDDIO_FPGA 10
+0V75_REF +0V75_REF 3,8,12
DGND 3,4,5,6,8,9,10,11,12
+1V5
C150 10uF
C151 2200nF
C152 1uF
C153 100nF
C155 10nF
+2V5
C199 1uF
C197 100nF
C195 10nF
+2V5
C162 10uF
C163 2200nF
C164 1uF
C165 100nF
C166 100nF
C167 10nF
C168 10nF
U6-1
EP4SGX110HF35C2N
+1V5
+1V5
R50 49.9
+0V75_REF
R51 49.9
DDR3_RDN
DDR3_RUP
VCCIO1A_1
VCCIO1A_2
VCCIO1A_3
VREFB1AN0
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RUP1A/DIFFIO_RX_L1P/DIFFOUT_L2P
IO_1A/DQS2L/DIFFIO_RX_L3P/DIFFOUT_L6P
IO_1A/DQSN2L/DIFFIO_RX_L3N/DIFFOUT_L6N
IO_1A/DQS1L/DIFFIO_RX_L2P/DIFFOUT_L4P
IO_1A/DQSN1L/DIFFIO_RX_L2N/DIFFOUT_L4N
IO_1A/DQ4L/DIFFIO_RX_L7P/DIFFOUT_L14P
IO_1A/DQ2L/DIFFIO_RX_L4P/DIFFOUT_L8P
IO_1A/DQ2L/DIFFIO_RX_L4N/DIFFOUT_L8N
IO_1A/DQS4L/DIFFIO_RX_L6P/DIFFOUT_L12P
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IO_1A/DQ1L/DIFFIO_TX_L2N/DIFFOUT_L3N
IO_1A/DIFFIO_TX_L1P/DIFFOUT_L1P
IO_1A/DQ1L/DIFFIO_TX_L2P/DIFFOUT_L3P
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IO_1A/DIFFIO_TX_L8P/DIFFOUT_L15P
IO_1A/DQ3L/DIFFIO_TX_L5P/DIFFOUT_L9P
IO_1A/DQ3L/DIFFIO_TX_L5N/DIFFOUT_L9N
DDR3_G0_DQS0_P
DDR3_G0_DQ7
DDR3_G0_DQ5
DDR3_G0_DQ4
DDR3_G0_DM0
DDR3_G0_DQ1
DDR3_G0_DQS0_N
DDR3_G0_DQ6
DDR3_G0_DQ2
DDR3_G0_DQ0
DDR3_G0_DQ3
VCCIO1C_1
VCCIO1C_2
CLK0N_DIFFIO_RX_L14N_DIFFOUT_L28N
CLK0P_DIFFIO_RX_L14P_DIFFOUT_L28P
CLK1N
CLK1P
VREFB1CN0
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IO_1C/DQS5L/DIFFIO_RX_L9P/DIFFOUT_L18P
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IO_1C/DQ5L/DIFFIO_RX_L10N/DIFFOUT_L20N
IO_1C/DQ5L/DIFFIO_TX_L10P/DIFFOUT_L19P
IO_1C/DIFFIO_TX_L9P/DIFFOUT_L17P
IO_1C/DIFFIO_TX_L9N/DIFFOUT_L17N
CK_GX_TX_MCLK
CK_GX_RX_MCLK_FB
CK_GX_TX_MCLK_FB
CK_GX_RX_MCLK
GX_TX_RESET_L
GX_RX_RESET_L
GX_RECLK_EN
DWIRE
DDR3_SCLK
DDR3_SDATA
DDR3_EVENT_L
Extra 1C pins on Sh 9
U6-3
EP4SGX110HF35C2N
+2V5
VCCIO3A_1
VCCIO3A_2
VCCIO3A_3
VCCIO3A_4
VREFB3AN0
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RUP3A/DIFFIO_RX_B1P/DIFFOUT_B2P/DQS1B
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IO_3A/DQ8B/DIFFOUT_B15N
IO_3A/DQ4B/DIFFOUT_B11P
IO_3A/DQ4B/DIFFOUT_B11N
IO_3A/DQ3B/DIFFOUT_B9P
IO_3A/DQ2B/DIFFOUT_B13P
IO_3A/DQ5D/DIFFOUT_B15P
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IO_3A/DQ1B/DIFFOUT_B3P
IO_3A/DQ1B/DIFFOUT_B1P
IO_3A/DQ1B/DIFFOUT_B1N
DEMO3_DIO_RESET_L
DEMO3_PAR_FRAMEVALID
LA_DATA20
LA_DATA19
LA_DATA18
LA_DATA21
LA_DATA16
LA_DATA17
LA_DATA23
LA_DATA22
LA_DATA2
LA_DATA27
LA_DATA25
LA_DATA24
LA_DATA6
LA_DATA26
LED_GRN0
LED_RED0
LED_GX_GRN
LED_GX_RED
LED_MAIN_ENABLE
LED_VDDIO_ENABLE
DEMO3_DIO_SPARE3
DEMO3_PAR_PIXCLK
DEMO3_PAR_DATA3
DEMO3_PAR_DATA13
DEMO3_DIO_SPARE2
DEMO3_PAR_DATA9
DEMO3_DIO_SPARE0
DEMO3_PAR_LINEVALID
DEMO3_DIO_SPARE4
DEMO3_PAR_DATA1
DEMO3_PAR_DATA5
DEMO3_PAR_DATA7
DEMO3_PAR_DATA11
DEMO3_PAR_DATA15
DEMO3_I2C_SCLK
DEMO3_I2C_SDATA
VCCIO3C_1
VCCIO3C_2
CLK4P_DIFFIO_RX_B16P_DIFFOUT_B32P
CLK4N_DIFFIO_RX_B16N_DIFFOUT_B32N
CLK5P_DIFFOUT_B31P
CLK5N_DIFFOUT_B31N
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IO_3C/PLL_B1_FBP/CLKOUT1/DIFFIO_RX_B15P/DIFFOUT_B30P
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IO_3CD08B/DIFFOUT_B25N
IO_3C/DQS8B/DIFFIO_RX_B12P/DIFFOUT_B24P
IO_3C/DQS7B/DIFFIO_RX_B11P/DIFFOUT_B22P
IO_3C/DQ8B/DIFFIO_RX_B13P/DIFFOUT_B26P
IO_3C/DQSN8B/DIFFIO_RX_B12N/DIFFOUT_B24N
IO_3C/DQSN7B/DIFFIO_RX_B11N/DIFFOUT_B22N
IO_3C/DQ8B/DIFFIO_RX_B13N/DIFFOUT_B26N
IO_3C/DQ7B/DIFFOUT_B23P
IO_3C/DQ7B/DIFFOUT_B23N
IO_3C/DQ7B/DIFFOUT_B21N
IO_3C/DQ7B/DIFFOUT_B21P
CK_DEMO3_MCLK
CK_DEMO3_MCLK_FB
LA_DATA31
PLL_LOOP
LA_DATA30
LA_DATA29
LA_DATA28
LA_DATA15
LA_DATA4
LA_DATA0
LA_DATA10
LA_DATA8
LA_DATA14
LA_DATA12
LED_HB_ENABLE
LED_FPGA_ENABLE
DEMO3_DIO_SPARE5
CLK_FPGA_EN
U6-2
EP4SGX110HF35C2N
+2V5
VCCIO2A_1
VCCIO2A_2
VCCIO2A_3
VREFB2AN0
RUP2A/DIFFIO_RX_L28P/DIFFOUT_L55P
RDN2A/DIFFIO_RX_L28N/DIFFOUT_L55N
IO_2A/DQ14L/DIFFIO_TX_L27N/DIFFOUT_L54N
IO_2A/DQ14L/DIFFIO_TX_L27P/DIFFOUT_L54P
IO_2A/DIFFIO_TX_L28N/DIFFOUT_L56N
IO_2A/DIFFIO_TX_L28P/DIFFOUT_L56P
IO_2A/DIFFIO_TX_L21N/DIFFOUT_L42N
IO_2A/DIFFIO_TX_L21P/DIFFOUT_L42P
IO_2A/DQ14L/DIFFIO_TX_L26N/DIFFOUT_L52N
IO_2A/DQ14L/DIFFIO_TX_L26P/DIFFOUT_L52P
IO_2A/DQ12L/DIFFIO_TX_L23N/DIFFOUT_L46N
IO_2A/DQ11L/DIFFIO_TX_L22N/DIFFOUT_L44N
IO_2A/DQ12L/DIFFIO_TX_L24P/DIFFOUT_L48P
IO_2A/DQ12L/DIFFIO_TX_L24N/DIFFOUT_L48N
IO_2A/DIFFIO_RX_L21N/DIFFOUT_L41N
IO_2A/DQ12L/DIFFIO_TX_L23P/DIFFOUT_L46P
IO_2A/DQ11L/DIFFIO_TX_L22P/DIFFOUT_L44P
IO_2A/DQ13L/DIFFIO_TX_L25P/DIFFOUT_L50P
IO_2A/DQ13L/DIFFIO_TX_L25N/DIFFOUT_L50N
IO_2A/DIFFIO_RX_L21P/DIFFOUT_L41P
IO_2A/DQS11L/DIFFIO_RX_L23P/DIFFOUT_L45P
IO_2A/DQS12L/DIFFIO_RX_L24P/DIFFOUT_L47P
IO_2A/DQSN12L/DIFFIO_RX_L24N/DIFFOUT_L47N
IO_2A/DQ11L/DIFFIO_RX_L22P/DIFFOUT_L43P
IO_2A/DQSN11L/DIFFIO_RX_L23N/DIFFOUT_L45N
IO_2A/DQ13L/DIFFIO_RX_L25P/DIFFOUT_L49P
IO_2A/DQ13L/DIFFIO_RX_L25N/DIFFOUT_L49N
IO_2A/DQ11L/DIFFIO_RX_L22N/DIFFOUT_L43N
IO_2A/DQSN14L/DIFFIO_RX_L27N/DIFFOUT_L53N
IO_2A/DQS14L/DIFFIO_RX_L27P/DIFFOUT_L53P
IO_2A/DQS13L/DIFFIO_RX_L26P/DIFFOUT_L51P
IO_2A/DQSN13L/DIFFIO_RX_L26N/DIFFOUT_L51N
SER_TX0_GPIO0
SER_TX0_GPIO1
GX_RX_SPARE8
GX_RX_SPARE7
GX_RX_SPARE6
GX_RX_SPARE5
SER_TX0_HS_CLK0_N
SER_TX0_HS_CLK0_P
GX_RX_SPARE4
GX_RX_SPARE3
SER_TX0_HS_DATA3_N
SER_TX0_HS_DATA2_N
SER_TX0_HS_DATA0_P
SER_TX0_HS_DATA0_N
GX_RX_SPARE2
SER_TX0_HS_DATA3_P
SER_TX0_HS_DATA2_P
SER_TX0_HS_DATA1_P
SER_TX0_HS_DATA1_N
GX_RX_SPARE1
GX_RX_SPARE13
SER_TX0_LP_CLKP0
SER_TX0_LP_CLKN0
SER_TX0_LP_DATAP1
SER_TX0_LP_DATAP0
SER_TX0_LP_DATAN0
SER_TX0_LP_DATAN1
SER_TX0_LP_DATAN2
SER_TX0_LP_DATAP2
SER_TX0_LP_DATAP3
SER_TX0_LP_DATAN3
VCCIO2C_1
VCCIO2C_2
CLK2P_DIFFIO_RX_L15P_DIFFOUT_L29P
CLK2N_DIFFIO_RX_L15N_DIFFOUT_L29N
CLK3P
CLK3N
VREFB2CN0
IO_2C/DIFFIO_TX_L20P/DIFFOUT_L40P
IO_2C/DQ8L/DIFFIO_TX_L16P/DIFFOUT_L32P
IO_2C/DQ8L/DIFFIO_TX_L16N/DIFFOUT_L32N
IO_2C/DQ10L/DIFFIO_TX_L19N/DIFFOUT_L38N
IO_2C/DQ8L/DIFFIO_TX_L16P/DIFFOUT_L31P
IO_2C/DQ10L/DIFFIO_TX_L19P/DIFFOUT_L38P
IO_2C/DQS9L/DIFFIO_RX_L18P/DIFFOUT_L35P
IO_2C/DQ8L/DIFFIO_RX_L16N/DIFFOUT_L31N
IO_2C/DQS8L/DIFFIO_RX_L17P/DIFFOUT_L33P
IO_2C/DQSN8L/DIFFIO_RX_L18N/DIFFOUT_L35N
IO_2C/DQSN10L/DIFFIO_RX_L20N/DIFFOUT_L39N
IO_2C/DQSN8L/DIFFIO_RX_L17N/DIFFOUT_L33N
IO_2C/DQS10L/DIFFIO_RX_L20P/DIFFOUT_L39P
IO_2C/DQ10L/DIFFIO_RX_L19N/DIFFOUT_L37N
IO_2C/DQ10L/DIFFIO_RX_L19P/DIFFOUT_L37P
IO_2C/DIFFIO_TX_L15N/DIFFOUT_L30N
IO_2C/DQ9L/DIFFIO_TX_L17N/DIFFOUT_L34N
IO_2C/DIFFIO_TX_L15P/DIFFOUT_L30P
IO_2C/DQ9L/DIFFIO_TX_L17P/DIFFOUT_L34P
IO_2C/DQ9L/DIFFIO_TX_L18P/DIFFOUT_L36P
IO_2C/DQ9L/DIFFIO_TX_L18N/DIFFOUT_L36N
IO_2C/DIFFIO_TX_L20N/DIFFOUT_L40N
ID_Rx
ID_Tx
GX_RX_I2C_SCLK
GX_RX_I2C_SDATA
GX_TX_SPARE2
GX_TX_SPARE1
GX_RX_SPARE15
GX_RX_SPARE14
GX_RX_SPARE12
GX_RX_SPARE0
GX_RX_SPARE10
GX_RX_SPARE11
GX_RX_SPARE9
GX_TX_SPARE0
GX_TX_SPARE6
GX_TX_SPARE8
GX_TX_SPARE7
GX_TX_SPARE11
GX_TX_SPARE5
GX_TX_SPARE4
GX_TX_SPARE3
R74 10K
R75 10K
R77 1.5K
R78 1.5K
U6-4
EP4SGX110HF35C2N
+2V5
VCCIO4A_1
VCCIO4A_2
VCCIO4A_3
VCCIO4A_4
VREFB4AN0
RUP4A/DIFFIO_RX_B32P/DIFFOUT_B63P/DQS17B
RDN4A/DIFFIO_RX_B32N/DIFFOUT_B63N/DQSN17B
IO_4A/DIFFIO_RX_B23P/DIFFOUT_B45P
IO_4A/DIFFOUT_B46P
IO_4A/DIFFIO_RX_B23N/DIFFOUT_B45N
IO_4A/DIFFOUT_B46N
IO_4A/DQ14B/DIFFOUT_B54P
IO_4A/DQ14B/DIFFOUT_B54N
IO_4A/DQ14B/DIFFIO_RX_B27P/DIFFOUT_B53P
IO_4A/DQS14B/DIFFIO_RX_B28P/DIFFOUT_B55P
IO_4A/DQ15B/DIFFOUT_B56P
IO_4A/DQ13B/DIFFOUT_B50P
IO_4A/DQ14B/DIFFIO_RX_B27N/DIFFOUT_B53N
IO_4A/DQSN14B/DIFFIO_RX_B28N/DIFFOUT_B55N
IO_4A/DQ15B/DIFFOUT_B56N
IO_4A/DQ13B/DIFFOUT_B52P
IO_4A/DQS15B/DIFFIO_RX_B29P/DIFFOUT_B57P
IO_4A/DQS13B/DIFFIO_RX_B26P/DIFFOUT_B51P
IO_4A/DQ13B/DIFFOUT_B52N
IO_4A/DQ13B/DIFFOUT_B50N
IO_4A/DQ15B/DIFFOUT_B58N
IO_4A/DQ15B/DIFFOUT_B58P
IO_4A/DQSN15B/DIFFIO_RX_B29N/DIFFOUT_B57N
IO_4A/DQSN13B/DIFFIO_RX_B26N/DIFFOUT_B51N
IO_4A/DQ12B/DIFFOUT_B48P
IO_4A/DQ16B/DIFFOUT_B60P
IO_4A/DQS12B/DIFFIO_RX_B25P/DIFFOUT_B49P
IO_4A/DQ12B/DIFFIO_RX_B24P/DIFFOUT_B47P
IO_4A/DQ17B/DIFFOUT_B62P
IO_4A/DQS16B/DIFFIO_RX_B31P/DIFFOUT_B61P
IO_4A/DQ16B/DIFFIO_RX_B30P/DIFFOUT_B59P
IO_4A/DQ16B/DIFFOUT_B60N
IO_4A/DQSN12B/DIFFIO_RX_B25N/DIFFOUT_B49N
IO_4A/DQ12B/DIFFIO_RX_B24N/DIFFOUT_B47N
IO_4A/DQ12B/DIFFOUT_B48N
IO_4A/DQ17B/DIFFOUT_B64P
IO_4A/DQ17B/DIFFOUT_B64N
IO_4A/DQ17B/DIFFOUT_B62N
IO_4A/DQSN16B/DIFFIO_RX_B31N/DIFFOUT_B61N
IO_4A/DQ16B/DIFFIO_RX_B30N/DIFFOUT_B59N
SER_RX0_LP_CLKP0
SER_RX0_LP_CLKN0
HB_PWR_ENABLE
LA_DATA9
LA_DATA13
LA_DATA11
SER_RX5_GPIO1
SER_RX4_GPIO0
LA_DATA5
LA_DATA7
SER_RX1_GPIO1
SER_RX5_GPIO0
SER_RX4_GPIO1
PF_HB_L
SER_RX1_GPIO0
SER_RX3_GPIO1
SER_RX0_GPIO0
SER_RX2_GPIO0
LA_DATA1
LA_DATA3
SER_RX3_GPIO0
SER_RX0_GPIO1
DEMO3_PAR_DATA8
SER_RX2_GPIO1
DEMO3_DIO_SPARE1
DEMO3_PAR_DATA12
SER_RX1_LP_CLKP1
DEMO3_PAR_DATA2
DEMO3_PAR_DATA4
DEMO3_PAR_DATA0
DEMO3_PAR_DATA6
DEMO3_PAR_DATA10
DEMO3_PAR_DATA14
VDDQ_PGOOD
SER_RX1_LP_CLKN1
Rev ID
VCCIO4C_1
VCCIO4C_2
CLK6P_DIFFIO_RX_B17P_DIFFOUT_B33P
CLK6N_DIFFIO_RX_B17N_DIFFOUT_B33N
CLK7P_DIFFOUT_B34P
CLK7N_DIFFOUT_B34N
VREFB4CN0
IO_4C/DQ9B/DIFFOUT_B38P
IO_4C/DQS9B/DIFFIO_RX_B19P/DIFFOUT_B37P
IO_4C/DIFFIO_RX_B18P/DIFFOUT_B35P
IO_4C/DQSN9B/DIFFIO_RX_B19N/DIFFOUT_B37N
IO_4C/DIFFIO_RX_B18N/DIFFOUT_B35N
IO_4C/DQ9B/DIFFOUT_B36P
IO_4C/DQ9B/DIFFOUT_B36N
IO_4C/DQS11B/DIFFIO_RX_B22P/DIFFOUT_B43P
IO_4C/DQS10B/DIFFIO_RX_B21P/DIFFOUT_B41P
IO_4C/DQ9B/DIFFOUT_B38N
IO_4C/DQSN11B/DIFFIO_RX_B22N/DIFFOUT_B43N
IO_4C/DQSN10B/DIFFIO_RX_B21N/DIFFOUT_B41N
IO_4C/DQ10B/DIFFIO_RX_B20P/DIFFOUT_B39P
IO_4C/DQ10B/DIFFOUT_B40N
IO_4C/DQ11B/DIFFOUT_B42P
IO_4C/DQ11B/DIFFOUT_B42N
IO_4C/DQ10B/DIFFIO_RX_B20N/DIFFOUT_B39N
IO_4C/DQ10B/DIFFOUT_B40P
IO_4C/DQ11B/DIFFOUT_B44P
IO_4C/DQ11B/DIFFOUT_B44N
CK_HB_MCLK_FB
CK_34MHZ_FPGA_P
CK_34MHZ_FPGA_N
R82 100
HB_DIO_SPARE0
HB_DIO_SPARE1
HB_DIO_SPARE2
HB_DIO_SPARE3
HB_DIO_SPARE4
HB_DIO_SPARE5
HB_DIO_SPARE6
HB_DIO_SPARE7
HB_DIO_SPARE8
HB_DIO_SPARE9
HB_DIO_SPARE10
HB_DIO_SPARE11
HB_DIO_RESET_L
CK_HB_MCLK
PLL_LOOP
HB_I2C_SCLK
HB_I2C_SDATA
+VDDIO_FPGA
HB_I2C_SCLK R79 1.5K
HB_I2C_SDATA R80 1.5K
C157 1uF
C158 100nF
C159 100nF
C160 10nF
C161 10nF
C192 1uF
C193 100nF
C194 10nF
C189 1uF
C190 100nF
C191 10nF
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Size C
Document Name AP21088-FrameBuffer_Demo
Rev 1
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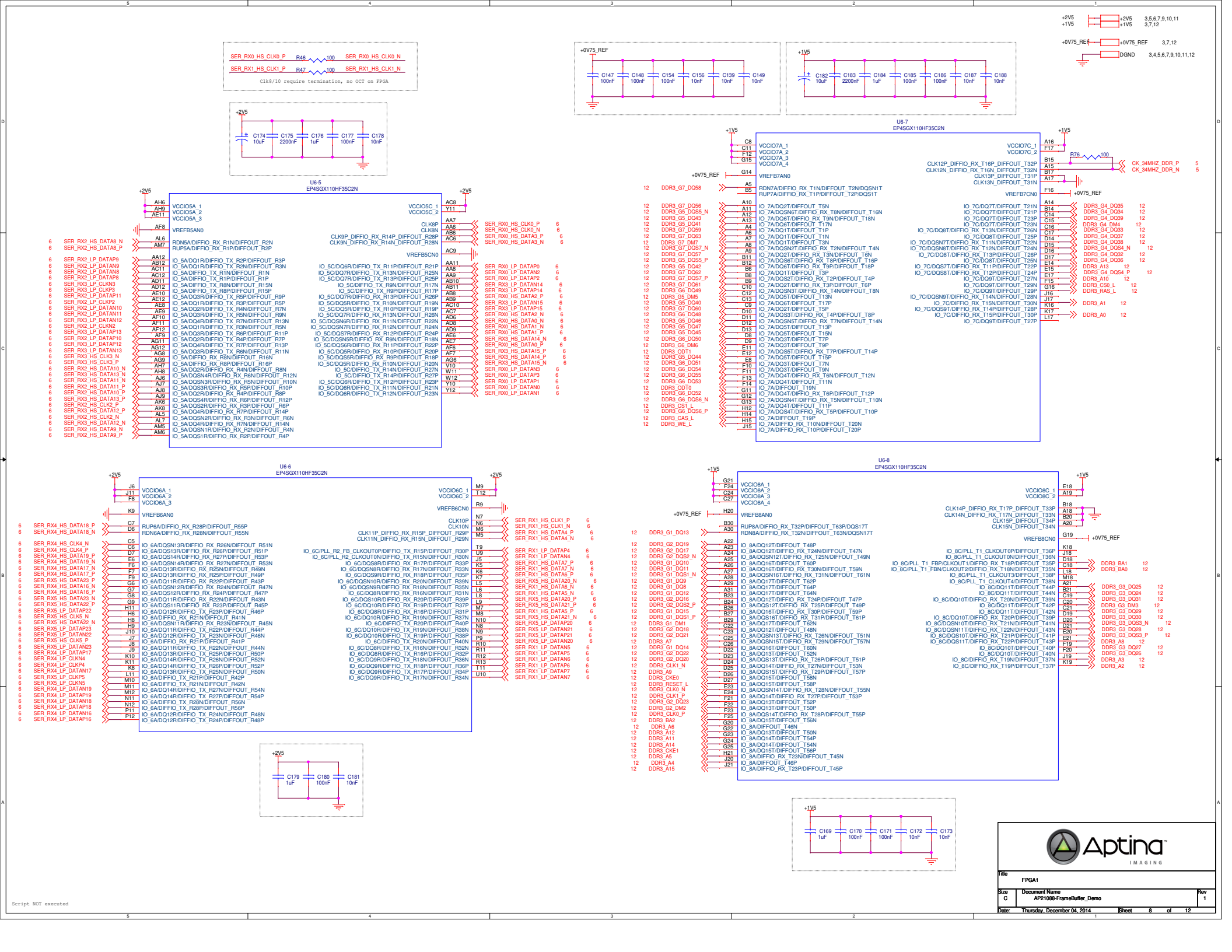
+2V5 +1V5 +2V5 3,5,6,7,9,10,11
+1V5 3,7,12
+0V75_REF +0V75_REF 3,7,12
DGND 3,4,5,6,7,9,10,11,12
SER_RX0_HS_CLK0_P R46 100 SER_RX0_HS_CLK0_N
SER_RX1_HS_CLK1_P R47 100 SER_RX1_HS_CLK1_N
Clk8/10 require termination, no OCT on FPGA
+0V75_REF C147 100nF C148 100nF C154 100nF C156 10nF C139 10nF C149 10nF
+1V5 C182 10uF C183 2200nF C184 1uF C185 100nF C186 100nF C187 10nF C188 10nF
+2V5 C174 10uF C175 2200nF C176 1uF C177 100nF C178 10nF
U6-5
EP4SGX110HF35C2N
U6-7
EP4SGX110HF35C2N
U6-6
EP4SGX110HF35C2N
U6-8
EP4SGX110HF35C2N
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Size C Document Name AP21088-FrameBuffer_Demo Rev 1
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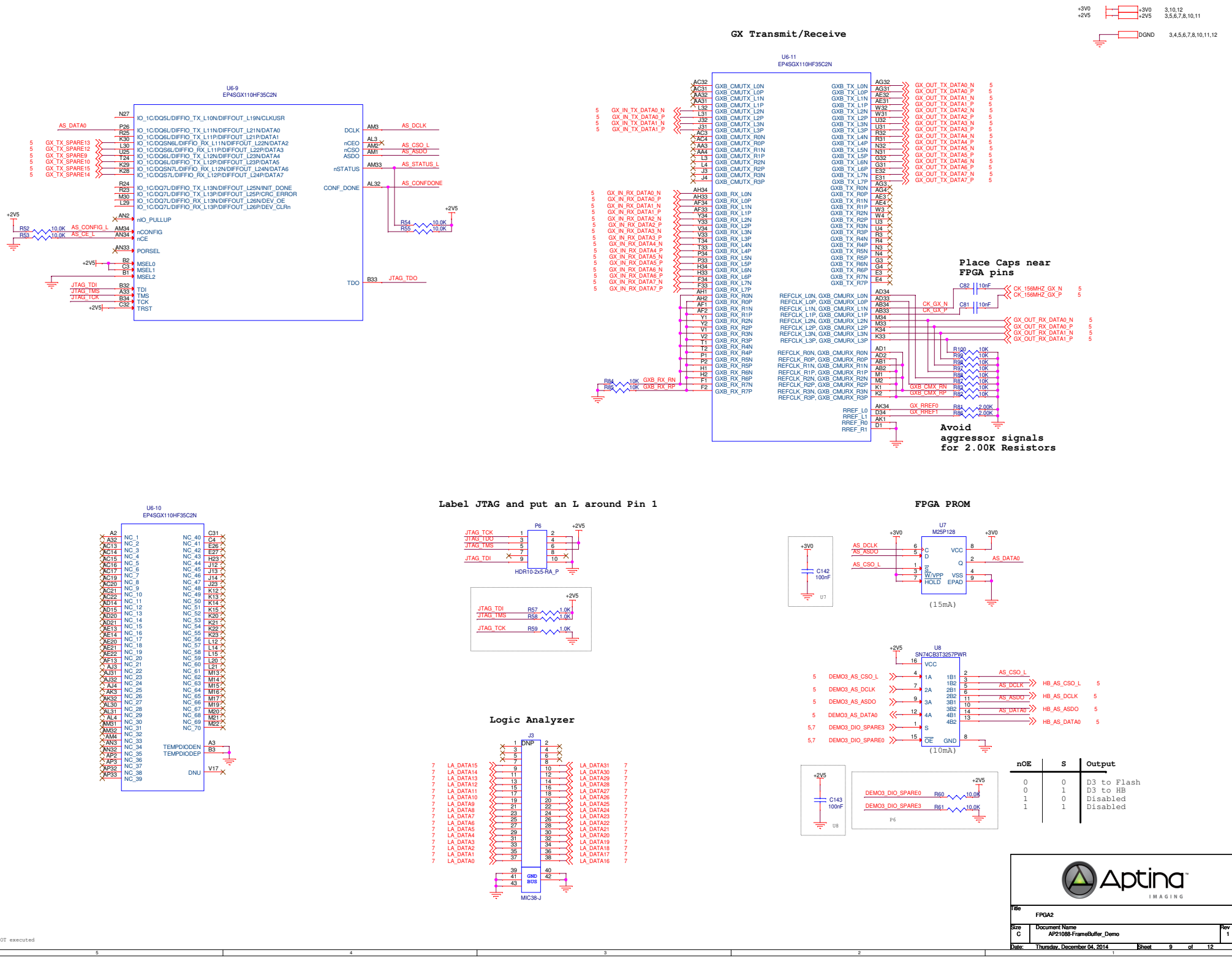
+3V0
+2V5
3,10,12
3,5,6,7,8,10,11
DGND
3,4,5,6,7,8,10,11,12
GX Transmit/Receive
U6-9
EP4SGX110HF35C2N
U6-11
EP4SGX110HF35C2N
Place Caps near
FPGA pins
Avoid
aggressor signals
for 2.00K Resistors
U6-10
EP4SGX110HF35C2N
Label JTAG and put an L around Pin 1
HDR10-2x5-RA_P
FPGA PROM
U7
M25P128
(15mA)
U8
SN74CB3T3257PWR
(10mA)
Logic Analyzer
J3
DNP
MIC38-J
nOE
S
Output
0
0
D3 to Flash
0
1
D3 to HB
1
0
Disabled
1
1
Disabled
Aptina
IMAGING
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FPGA2
Size
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Document Name
AP21088-FrameBuffer_Demo
Rev
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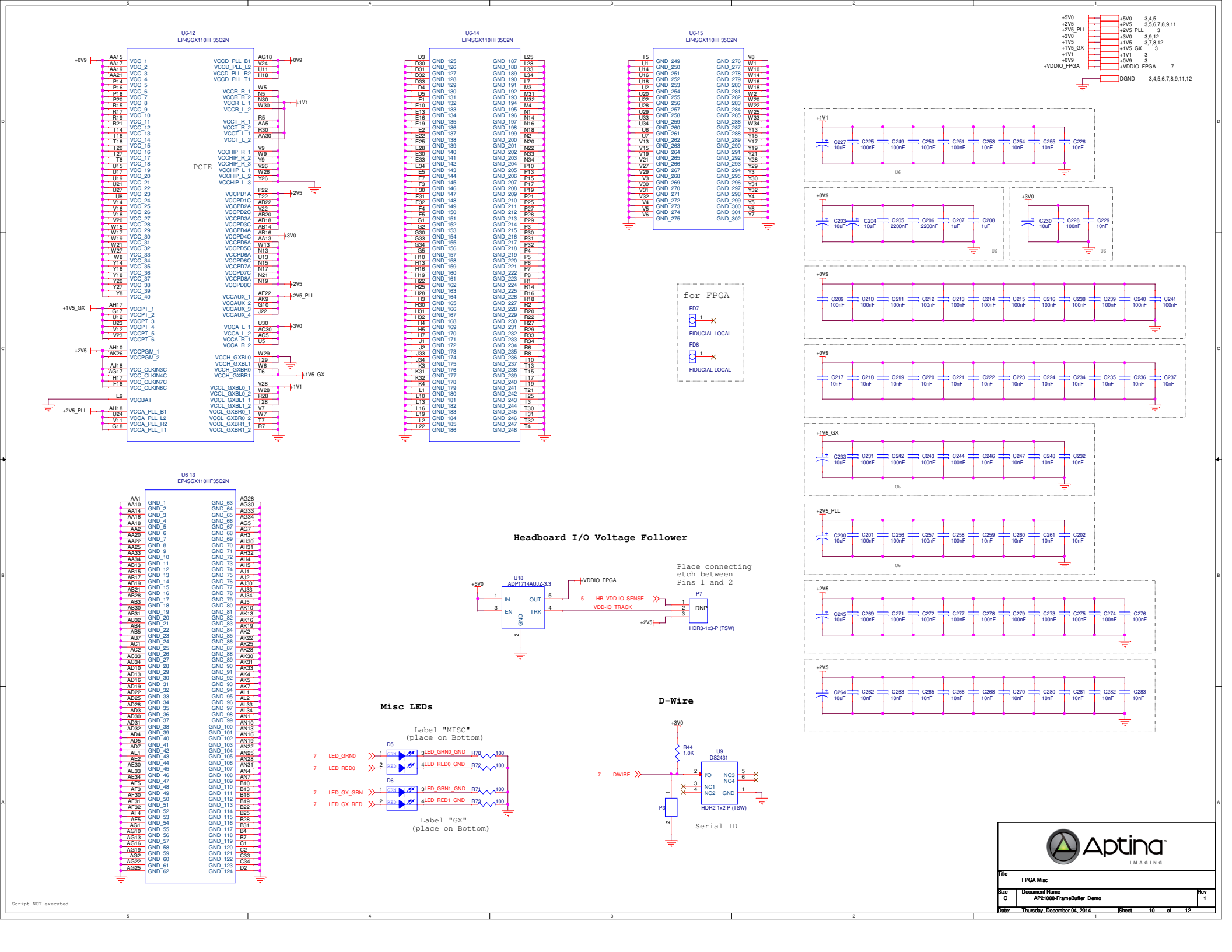
U6-12
EP4SGX110HF35C2N
PCIE
U6-14
EP4SGX110HF35C2N
U6-15
EP4SGX110HF35C2N
U6-13
EP4SGX110HF35C2N
for FPGA
FD7
FIDUCIAL-LOCAL
FD8
FIDUCIAL-LOCAL
Headboard I/O Voltage Follower
U18
ADP1714AUJZ-3.3
P7
DNP
HDR3-1x3-P (TSW)
HB_VDD-IO_SENSE
VDD-IO_TRACK
Place connecting
etch between
Pins 1 and 2
Misc LEDs
Label "MISC"
(place on Bottom)
Label "GX"
(place on Bottom)
D-Wire
U9
DS2431
HDR2-1x2-P (TSW)
Serial ID
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Aptina
IMAGING
Title
FPGA Misc
Size
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Document Name
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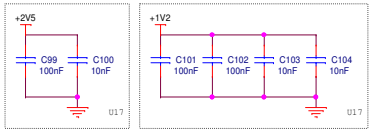

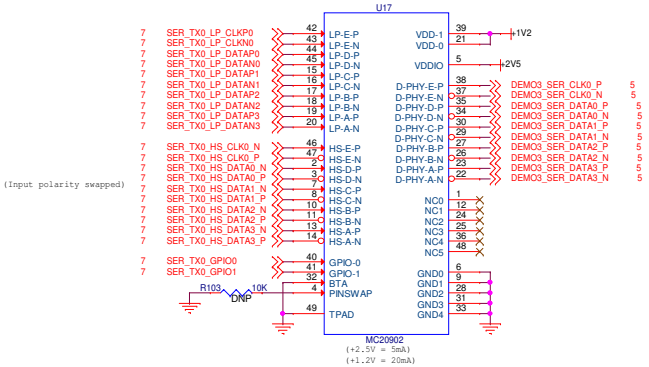

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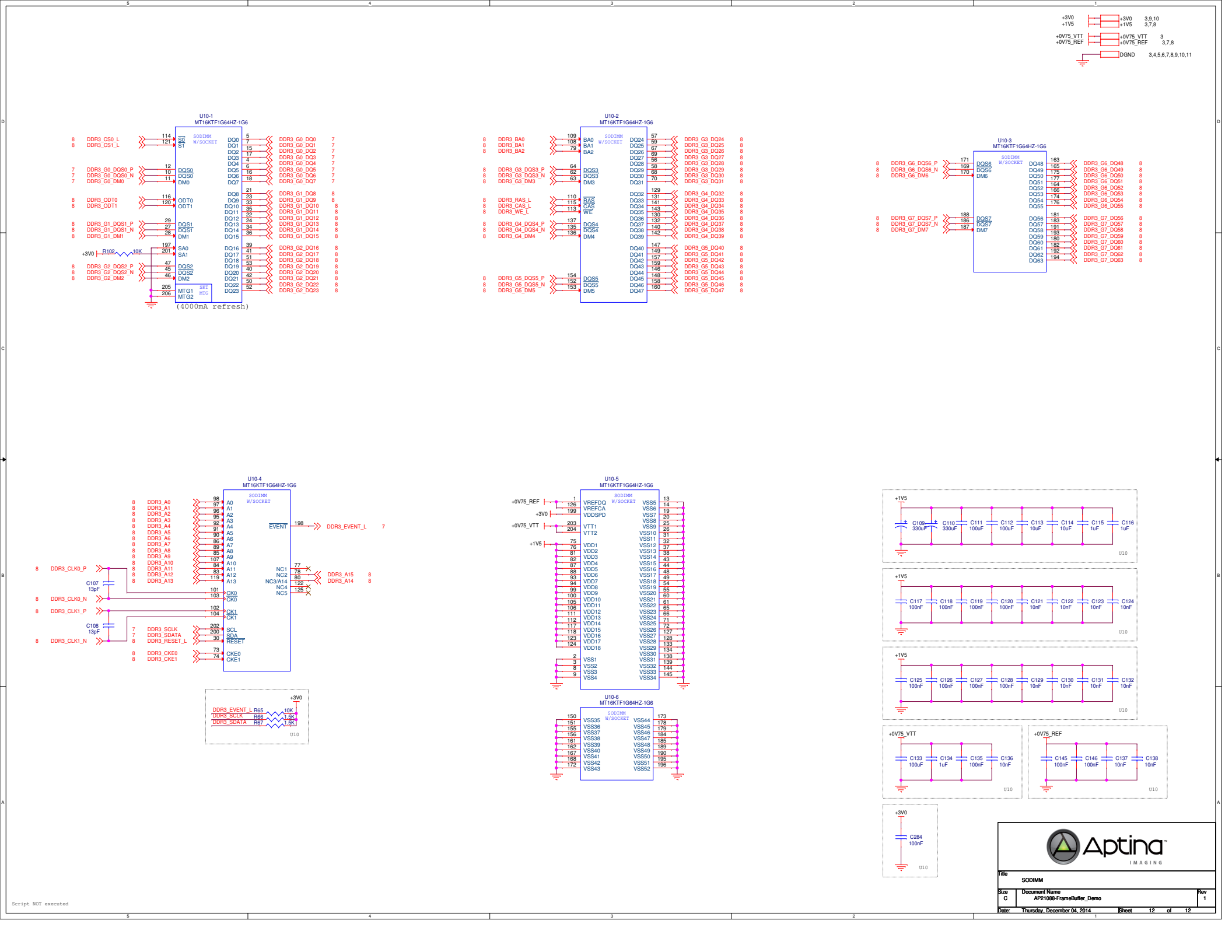
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+0V75_VTT +0V75_REF +0V75_VTT +0V75_REF 3 3,7,8
DGND 3,4,5,6,7,8,9,10,11
U10-1 MT16KTF1G64HZ-1G6
SODIMM W/SOCKET
(4000mA refresh)
U10-2 MT16KTF1G64HZ-1G6
U10-3 MT16KTF1G64HZ-1G6
U10-4 MT16KTF1G64HZ-1G6
U10-5 MT16KTF1G64HZ-1G6
U10-6 MT16KTF1G64HZ-1G6
Aptina IMAGING
Title SODIMM
Size C Document Name AP21088-FrameBuffer_Demo Rev 1
Date: Thursday, December 04, 2014 Sheet 12 of 12
Script NOT executed